2 f

1

. A method for power gating a downlink beam

2 frame signal, the method comprising:

transmitting, to form a single frame, at least a

4 first header signal, a first payload signal, a second

5 header signal, and a second/payload signal;

6 when a power gating signal is active, removing RF

7 power from at least one of the first header signal and

8 first payload signal /in combination, and the second

9 header signal and second payload signal in

10 combination, thereby reducing DC power consumption.

1 2. The method of claim 1, further comprising

2 hopping the downlink beam frame signal between at

3 least two terrestrial cells.

1 3. The /method of claim 2, further comprising

2 the step of \int activating the power gating signal based

3 on the terrestrial cell to which the downlink beam

4 frame signal is currently hopped.

- 23 -

- 1 4. The method of claim 1, further comprising
- 2 the step of activating the power gating signal based
- 3 on a statistical multiplexing estimate of downlink
- 4 frame utilization.
- 1 5. The meth ϕ d of claim 1, further comprising
- 2 the step of activating the power gating signal in
- 3 order to maintai \hbar at least one data queue on average
- 4 approximately at preselected occupancy level.
- 1 6. The method of claim 1, further comprising
- 2 the step of transmitting a first flush signal and a
- 3 second flush signal, and wherein removing power
- 4 comprises removing power from at least one of the
- 5 first header signal, first payload signal, and first
- 6 flush signal in combination, and the second header
- 7 signal, second payload signal, and second flush signal
- 8 in combination.
- 1 \bigcirc The method of claim 1, wherein removing
- 2 power for the first header signal, the first payload
- 3 signal, the second header signal, and the second
- 4 payload signal.

- 24 -

- 1 8. The method of claim 1, wherein removing
- 2 power comprises removing power from the first payload
- 3 signal, the second header signal, and the second
- 4 payload signal.
- 1 9. The method of claim 1, wherein removing
- 2 power comprises removing power from the first header
- 3 signal, the first payload signal, and the second
- 4 payload signal.
- 1 10. The method of/claim 1, wherein transmitting
- 2 comprises transmitting to form a single frame a first
- 3 header signal, a first payload signal, a second header
- 4 signal, a second payload signal, at least one
- 5 additional header signal, and at least one additional
- 6 payload signal;
- 7 when the power gating signal is active, removing
- 8 power from at least one of the first header signal and
- 9 first payload signal in combination, the second header
- 10 signal and second payload signal in combination, and
- 11 the additional header signal and the additional
- 12 payload signal in combination.

modulator.

6

- 25 -

1/. A power gating modyle for power gating a 1 downlink beam frame signal, the power gating module 2 3 comprising: a power amplifier for amplifying for transmission 4 including at least a first frame signals 5 signal, a first pay/load signal, a second header 6 signal, and a second payload signal; 7 a power gating circuit coupled to the power 8 amplifier, the power gating circuit including a power 9 gate input and pesponsive to a power gating signal to 10 remove power ffrom at least one of the first header 11 signal and first payload signal in combination, and 12 the second header signal and second payload signal in 13 combination before amplification by the power 14 amplifier, 15 The power gating module of claim 11, wherein 1 12./ the power gating circuit comprises a digital modulator 2 with a gating control input connected to the power 3 gate/input and a bandpass filter with a predetermined 4 passband coupled to a modulator output of the digital 5



- 26 -

- 1 13. The power gating module of claim 12, wherein
- 2 the digital modulator outputs a modulated signal with
- 3 frequency content outside the passband in response to
- 4 the power gating signal.
- 1 14. The power gating module of claim 13, wherein
- 2 the frequency content/is substantially DC frequency
- 3 content.
- 1 15. The power gating module of claim 12, wherein
- 2 the digital modulator is a QPSK modulator and further
- 3 comprising an /Inphase gate and a Quadrature gate
- 4 coupled to the digital modulator.
- 1 16. The power gating module of claim 15, wherein
- 2 the Inphase gate and the Quadrature gate are held in a
- 3 known output state in response to the power gating
- 4 signal.
- 1 17. The power gating module of claim 11, wherein
- 2 the power gating signal is active during the first
- 3 header signal, the first payload signal, the second
- 4 header signal, and the second payload signal.



- 1 18. The power gating module of claim 11, wherein
- 2 the power gating signal is active during the first
- 3 payload signal, the second header signal, and the
- 4 second payload signal.
- 1 19. The power gating module of claim 11, wherein
- 2 the power gating signal is active during the first
- 3 header signal, the first payload signal, and the
- 4 second payload signal.
- 1 20. The power /gating module of claim 11,
- 2 comprising:
- a switch coupled to the power amplifier, the
- 4 switch including /a feed path selection input;
- a first feed path coupled to the switch and
- 6 characterized/by a first hop location; and
- 7 a second feed path coupled to the switch and
- 8 characterized by a second hop location.
- 1 21. The power gating module of claim 20, wherein
- 2 the switch is a ferrite switch.

- 1 22. The power gating module of claim 20, wherein
- 2 the power gating signal is active based in part on the
- 3 feed path selection of the first hop location or the
- 4 second hop location.
- 1 22. A power gated frame signal comprising:
- a single frame comprising at least a first header
- 3 signal, a first payload signal, a second header
- 4 signal, and a second payload signal,
- 5 wherein at least one of the first header signal
- 6 and first payload/signal in combination, and the
- 7 second header signal and second payload signal in
- 8 combination is power gated.
- 1 24. The power gated frame signal of claim 23,
- 2 wherein the single frame further comprises at least
- 3 one additional header signal, and at least one
- 4 additional payload signal, and
- 5 wherein at least one of the first header signal
- 6 and first/payload signal in combination, the second
- 7 header signal and second payload signal in
- 8 combinat on, and the additional header signal and the

- 29 -

- 9 additional payload signal in combination is power 10 gated.
- 1 25. The power gating module of claim 23, wherein
- 2 the first header signal, the first payload signal, the
- 3 second header signal, and the second payload signal
- 4 are power gated.
- 1 26. The power gating module of claim 23, wherein
- 2 the first payload signal, the second header signal,
- 3 and the second payload signal are power gated.
- 1 27. The power gating module of claim 23, wherein
- 2 the first header signal, the first payload signal, and
- 3 the second payload signal are power gated.

(ild (2))